UNITED STATES PATENT APPLICATION

FOR

DELIVERING HIGH-CURRENT POWER AND GROUND VOLTAGES USING TOP SIDE OF CHIP PACKAGE SUBSTRATE

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SPECIFICATION

TITLE OF THE INVENTION

DELIVERING HIGH-CURRENT POWER AND GROUND VOLTAGES USING TOP SIDE OF CHIP PACKAGE SUBSTRATE

FIELD OF THE INVENTION

[0001] The present invention relates generally to interconnections between electronic packages and printed wiring boards. More specifically, the present invention relates to an interconnection system between a ball grid array package and a printed wiring board.

BACKGROUND OF THE INVENTION

[0002] Electronic systems generally include at least one printed wiring board (PWB) containing one or more integrated circuit (IC) chips or ICs. The IC may be packaged in a number of conventional ways. One prevalent IC package is known as a ball grid array (BGA) package. The name comes from the array of solder balls that are formed on the bottom of the package. The PWB has a corresponding array of pads to which the solder is bonded during the affixing of the BGA package to the PWB. The resulting interconnection is capable of serving a wide variety of applications.

[0003] Turning first to FIG. 1, a schematic diagram of two views of a conventional BGA package to PWB interconnection system 10 is shown. The schematic is not to scale. The upper view is a plan view and the lower view is an elevation view. The system 10 includes a BGA package 12 and a PWB 14. The BGA package 12 includes a chip 16, a package substrate 18, and

an array of a plurality of solder balls 19. The size, shape, type, and location of the chip 16 will depend on the circumstances but is generally centered on the package substrate 18. The size and shape of the package substrate 18 will depend on the circumstances but is generally rectangular and often square as shown. The size, number, and arrangement of the plurality of solder balls in the array 19 will depend on the circumstances but is generally formed of solder balls of uniform size in rectilinear rows and columns having uniform spacing or pitch in both directions.

[0004] In the electronics industry, improvements in functionality and performance are driving the demands for integration to unprecedented levels. With respect to the BGA package 12, the conventional response to the demands has been to increase the size of the package substrate 18, to shrink the pitch of the array 19, or both. These responses increase the number of contacts. Eventually a practical limit will be reached and a new approach will be desired. This is especially true given that higher current demands posed by the higher integration are eroding the relative contact gains of the conventional approach, that is, more and more of the new contacts are dedicated to power delivery and ground connections and not to signal communication.

BRIEF DESCRIPTION OF THE INVENTION

[0005] An electronic interconnection system for delivering high-current power and ground voltages using a non-bottom side of a chip package substrate is disclosed. The system includes a printed wiring board (PWB), a chip package, and a bridge lead. The PWB has at least a first and a second contact pad. The chip package includes a chip and a package substrate. The chip is mounted onto the package substrate and the package substrate has a bottom surface having at least a first contact pad and a second surface having at least a second contact pad. The first contact pad of the PWB and the first contact pad of the package substrate are coupled together. The bridge lead couples the second contact pad of the PWB with the second contact pad of the package substrate. The bridge lead may be selected from styles including flying lead, edge wiping, top wiping, and double wiping.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more exemplary embodiments of the present invention and, together with the detailed description, serve to explain the principles and exemplary implementations of the invention.

[0007] In the drawings:

FIG. 1 is a schematic diagram of two views of a conventional BGA package to PWB interconnection system;

FIG. 2 is a schematic diagram according to an embodiment of the present invention of two views of a BGA package to PWB interconnection system;

FIG. 3 is a schematic diagram according to the present invention of two views of an embodiment of the bridge leads of FIG. 2;

FIG. 4 is a schematic diagram according to the present invention of two views of an embodiment of the bridge leads of FIG. 2;

FIG. 5 is a schematic diagram according to the present invention of two views of an embodiment of the bridge leads of FIG. 2; and

FIG. 6 is a schematic diagram according to the present invention of two views of an embodiment of the bridge leads of FIG. 2.

DETAILED DESCRIPTION OF THE INVENTION

[0008] Various exemplary embodiments of the present invention are described herein in the context of a method and an apparatus for delivering high-current power and ground voltages using the top side of the chip package substrate. Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to exemplary implementations of the present invention as illustrated in the accompanying drawings. The same reference indicators will be used throughout the drawings and the following detailed descriptions to refer to the same or like parts.

[0009] In the interest of clarity, not all of the routine features of the exemplary implementations described herein are shown and described. It will of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the specific goals of the developer, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0010] Turning now to FIG. 2, a schematic diagram according to an embodiment of the present invention of two views of a BGA package to PWB interconnection system 20 is shown.

The system 20 is similar to the system 10 of FIG. 1 in that it includes the PWB 14 and the BGA package 12 having the chip 16, the package substrate 18, and the array of a plurality of solder balls 19. The discussion that follows will include references to the orientation shown in the figures, but the invention should not be limited to such orientations. In the system 10, the connections between the package substrate 18 and the PWB 14 are limited to the bottom plane of the package substrate 18. By contrast, the system 20 takes advantage of the fact that the package substrate 18 is three dimensional, that is, the system 20 includes connections to the package substrate 18 on more than the bottom surface. In the embodiment shown, a plurality of top-side contact pads 22 are provided on the package substrate 18. The number, size, shape, and location of the pads 22 will depend on the circumstances. Three of the pads 22 are shown connected to the PWB 14 through one or more bridge leads 24. In one embodiment, the leads 24 may be formed by the conventional wire bond technique. The leads 24 are shown only on the right and left sides of the plan view for greater clarity in the elevation view. In practice, any number of leads 24 could be connected to the various pads 22. In addition to the top side, it would also be possible to locate pads on the edges or vertical sides of the package substrate 18. Such edge pads might be limited to the edge or they might run from the top to the edge, from the bottom to the edge, from a first edge to a second edge, or from the top across the edge to the bottom. Edge pads are not shown in FIG. 2 in the interest of greater clarity.

[0011] Under the system 20, the connections provided by the various pads 22 and leads 24 could carry any of countless electrical signals. In one embodiment, the electrical signals are limited to those that have lower sensitivity to induced inductance such as constant voltages. For example, one or more of the pads 22 might be dedicated to the ground potential. Other pads 22

might be dedicated to higher potentials such as 1.2V, 1.5V, 1.8V, and the like. The addition of non-bottom-side connections not only increases the number of connections but could be used to free up bottom-side connections for more critical signals by moving less critical signals to the top side of the package substrate 18.

[0012] Turning now to FIG. 3, a schematic diagram according to the present invention of two views of an embodiment of the bridge leads 24 of FIG. 2 is shown. This particular embodiment will be referred to as the flying lead style of bridge lead 24. Only one pad 22 and one lead 24 are shown in the interest of greater clarity. In practice, any number of pads 22 and leads 24 might be used. The lead 24 is electrically connected to the package substrate 18 and the PWB 14. The exact size, shape, and placement of the lead 24 will depend on the circumstances. As indicated by a dashed line in the elevation view only, the lead 24 may be at least partially covered in an insulating material.

[0013] Turning now to FIG. 4, a schematic diagram according to the present invention of two views of an embodiment of the bridge leads 24 of FIG. 2 is shown. This particular embodiment will be referred to as the edge wiping style of bridge lead 24. The embodiment utilizes edge pads 22 as described above. Only two pads 22 and one lead 24 are shown in the interest of greater clarity. In practice, any number of pads 22 and leads 24 might be used. In the example shown, the lead 24 includes three spring type wipers 26 which might be wired separately internally to the lead 24. The lead 24 is electrically and mechanically connected to the PWB 14. For example, press fit pins could be used. The exact size, shape, and placement of the lead 24 will depend on the circumstances.

[0014] Turning now to FIG. 5, a schematic diagram according to the present invention of two views of an embodiment of the bridge leads 24 of FIG. 2 is shown. This particular embodiment will be referred to as the top wiping style of bridge lead 24. Only two pads 22 and one lead 24 are shown in the interest of greater clarity. In practice, any number of pads 22 and leads 24 might be used. In the example shown, the lead 24 includes two spring type wipers 26 which might be wired separately internally to the lead 24. The lead 24 is electrically and mechanically connected to the PWB 14. Again, for example, press fit pins could be used. The exact size, shape, and placement of the lead 24 will depend on the circumstances.

[0015] Turning now to FIG. 6, a schematic diagram according to the present invention of two views of an embodiment of the bridge leads 24 of FIG. 2 is shown. This particular embodiment will be referred to as the double wiping style of bridge lead 24. The upper view is a plan view with an optional heat sink removed. The outline of the package substrate 18 and a single pad 22 are shown in phantom for reference purposes as the lead 24 substantially dominates the plan view. By contrast, the chip 16 is visible through an optional window in the lead 24. The lower view is a cross sectional view along the line A-A with the optional heat sink installed. The system 20 includes the PWB 14, the chip 16, the package substrate 18, and one pad 22 similar to above. Only one pad 22 and one lead 24 are shown in the interest of greater clarity. In practice, any number of pads 22 and leads 24 might be used. Edge pads might also be used. The exact size, shape, and placement of the lead 24 will depend on the circumstances. In the example shown, the lead 24 includes at least one spring type double wiper 26. If more than one wiper 26 is provided, then each might be wired separately internally to the lead 24. The

wiper 26 is referred to as a double wiper because it presses against both the pad 22 and the PWB 14 which would be provided with a corresponding pad (not shown). Also shown in the cross sectional view are an optional heat sink 28 and a thermal interface material 30 to draw heat away from the chip 16. The heat sink 28 may be attached to the lead 24 by any suitable means of fastening including a screw as shown. Likewise, the lead 24 may be attached to the PWB 14 by any suitable means of fastening including a screw as shown. The body of the lead 24 alone or in combination with the heat sink 28 may be constructed in such a fashion as to serve as an Electro-Magnetic Interference (EMI) shield to the chip 16. For example, at least a portion of the outer surface of the body of the lead 24 could be coated with a conductive material and grounded as appropriate. The body of the lead 24 alone or in combination with the heat sink 28 may also be constructed in such a fashion as to provide structural support and/or protection for the chip 16 and package substrate 18.

[0016] Those of ordinary skill in the art will realize that the various styles of bridge lead embodiments presented above are not necessarily mutually exclusive. Which style of bridge lead or leads are used will depend in part on the circumstances.

[0017] While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.